CLAIMS

We claim:

1. A method for creating a clock signal distribution network on an integrated circuit layout, said method comprising:

determining a set of bounding box coordinates;

transforming said bounding box coordinates from a first coordinates system to a second coordinate system;

executing clock signal network generation code to generate a set of clock signal line coordinates;

transforming said set of clock signal line coordinates from said second coordinate system to a first coordinate system; and

rendering said transformed set of clock signal line coordinates in said first coordinate system.

2. The method for creating a clock signal distribution network on an integrated circuit layout as claimed in claim 1, said method further comprising:

repeating said steps of executing, transforming, and rendering.

3. The method for creating a clock signal distribution network on an integrated circuit layout as claimed in claim 1 wherein said clock signal network generation code generates a recursive "H" clock signal network.

4. The method for creating a clock signal distribution network on an integrated circuit layout as claimed in claim 1 wherein said clock signal network generation code generates a recursive “Y” clock signal network.

5. The method for creating a clock signal distribution network on an integrated circuit layout as claimed in claim 1, said method further comprising:

rendering shielding proximate to a root clock signal lines in said clock signal distribution network.

6. A clock signal distribution network on an integrated circuit layout, said clock signal distribution network comprising:

a recursive pattern of geometric shapes wherein each of said geometric shapes comprises

a root signal line;

a first leave line extending from a first end of said root signal line at a first non orthogonal angle to said root signal line;

a second leave line extending from a first end of said root signal line at a second non orthogonal angle to said root signal line;

a third leave line extending from a second end of said root signal line at a third non orthogonal angle to said root signal line; and

a fourth leave line extending from a second end of said root signal line at a fourth non orthogonal angle to said root signal line.

7. The clock signal distribution network on an integrated circuit layout as claimed in claim 6 wherein said first leave line and said second leave line are symmetrical about said root signal line.

8. The clock signal distribution network on an integrated circuit layout as claimed in claim 7 wherein said third leave line and said fourth leave line are symmetrical about said root signal line.

9. The clock signal distribution network on an integrated circuit layout as claimed in claim 6 wherein each geometric shape is coupled at a center of said root signal line.

10. The clock signal distribution network on an integrated circuit layout as claimed in claim 6 wherein said first leave line extends at a forty-five degree angle from said root signal line.

11. The clock signal distribution network on an integrated circuit layout as claimed in claim 6 wherein said first leave line extends at a sixty degree angle from said root signal line.

12. The clock signal distribution network on an integrated circuit layout as claimed in claim 6 wherein each of said leave lines is coupled to a local clock mesh network.

13. The clock signal distribution network on an integrated circuit layout as claimed in claim 6 further comprising:

a shielding structure proximate to said root signal line.

14. A clock signal distribution network on an integrated circuit layout, said clock signal distribution network comprising:

a series of parallel non Manhattan root clock signal lines; and

a series of local distribution structures coupled to said series of parallel non Manhattan root clock signal lines.

15. The clock signal distribution network on an integrated circuit layout as claimed in claim 14 further comprising:

a connection line connecting said series of parallel non Manhattan root clock signal lines.

16. The clock signal distribution network on an integrated circuit layout as claimed in claim 14 wherein said local distribution structures comprise an orthogonal cross structure.

17. The clock signal distribution network on an integrated circuit layout as claimed in claim 14 wherein said local distribution structures comprise clock signal lines that are orthogonal to said series of parallel non Manhattan root clock signal lines.

18. A clock signal distribution network on an integrated circuit layout, said clock signal distribution network comprising:

a collection of non Manhattan clock signal lines arranged to form a mesh.

19. The clock signal distribution network on an integrated circuit layout as claimed in claim 18 wherein said mesh further includes Manhattan clock signal lines.

20. The clock signal distribution network on an integrated circuit layout as claimed in claim 18 wherein said non Manhattan clock signal lines comprise forty-five degree lines.

21. The clock signal distribution network on an integrated circuit layout as claimed in claim 18 wherein said non Manhattan clock signal lines comprise sixty degree lines.

22. The clock signal distribution network on an integrated circuit layout as claimed in claim 18 wherein said mesh comprises coupled triangles.

23. The clock signal distribution network on an integrated circuit layout as claimed in claim 18 wherein said mesh comprises coupled hexagons.

24. The clock signal distribution network on an integrated circuit layout as claimed in claim 18 wherein said mesh is asymmetric.

25. The clock signal distribution network on an integrated circuit layout as claimed in claim 24 wherein said mesh comprises coupled triangles.

26. The clock signal distribution network on an integrated circuit layout as claimed in claim 24 wherein said mesh comprises coupled hexagons.

27. The clock signal distribution network on an integrated circuit layout as claimed in claim 18 further comprising:

a local clock signal distribution network coupled to said mesh, said local clock signal distribution network comprising non Manhattan wiring.

28. The clock signal distribution network on an integrated circuit layout as claimed in claim 27 wherein said local clock signal distribution network comprises a Y clock signal distribution network.

29. The clock signal distribution network on an integrated circuit layout as claimed in claim 23 wherein said local clock signal distribution network comprises a Y clock signal distribution network.

30. A method placing buffers for a clock signal distribution network, said method comprising:

routing a rough clock signal routing using non Manhattan wiring;

determining a length of wiring in said rough clock signal routing using non Manhattan wiring metrics; and

placing buffers as necessary as determined by said length of wiring.

31. The method placing buffers for a clock signal distribution network as claimed in claim 30, said method further comprising:

determining an area needed for clock signal distribution;

32. A method rendering a clock signal distribution network, said method comprising:

accepting a first parameter, said first parameter specifying a rotation value; and

rendering a clock signal network structure, said clock signal network structure orientation dependent on said rotation value.

33. The method rendering a clock signal distribution network as claimed in claim 32, said method further comprising:

accepting a second parameter said second parameter specifying a clock signal network structure type.

34. The method rendering a clock signal distribution network as claimed in claim 32 wherein said rotation value comprises a flag that specifies if a normal or rotated orientation should be rendered.

35. The method rendering a clock signal distribution network as claimed in claim 32 wherein said rotation value comprises a rotation angle that specifies a specific angle at which the clock signal network structure should be rendered.